WHAT IS CLAIMED IS:

1. A semiconductor package, comprising:

a die paddle defining multiple corners and opposed first and second surfaces;

at least one set of leads extending at least partially about the die paddle in spaced relation thereto, each of the leads having opposed first and second surfaces;

at least one tie bar attached to and extending from one of the corners of the die paddle, the tie bar having opposed first and second surfaces and at least one aperture disposed therein and extending between the first and second surfaces thereof;

a semiconductor die attached to the first surface of the die paddle and electrically connected to at least one of the leads; and

a package body at least partially covering the die paddle, the leads, the tie bar, and the semiconductor die such that the second surfaces of the leads are exposed in a common exterior surface of the package body, and a portion of the package body extends through the aperture of the tie bar.

2. The semiconductor package of Claim 1 wherein:

the die paddle has a quadrangular configuration defining four corners; and

four tie bars are attached to and extend diagonally from respective ones of the four corners of die paddle.

3. The semiconductor package of Claim 2 wherein:

each of the tie bars defines an outer end surface; and

the at least one aperture of each of the tie bars is disposed in close proximity to the outer end surface thereof.

4. The semiconductor package of Claim 3 wherein:

the package body defines four chamfers; and

the outer end surface of each of the tie bars extends to a respective one of the chamfers.

5. The semiconductor package of Claim 4 wherein:

each of the tie bars includes a plurality of apertures disposed therein;

portions of the package body extend through each of the apertures of each of the tie bars; and

one of the apertures of each of the tie bars is disposed in close proximity to the outer end surface thereof.

6. The semiconductor package of Claim 5 wherein:

the first and second surfaces of the die paddle are each generally planar;

the die paddle includes an etched surface which circumvents the second surface thereof;

the first and second surfaces of each of the tie bars are each generally planar;

the first surface of each of the tie bars extends in substantially co-planar relation to the first surface of the die paddle; and

the second surface of each of the tie bars extends in substantially co-planar relation to the etched surface of the die paddle.

7. The semiconductor package of Claim 6 wherein:

the first and second surfaces of each of the leads are each generally planar;

the first surface of each of the leads extends in substantially co-planar relation to the first surface of the die paddle;

the second surface of each of the leads extends in substantially co-planar relation to the second surface of the die paddle; and

the second surfaces of the leads and the second surface of the die paddle are exposed in and substantially flush with the exterior surface of the package body.

8. The semiconductor package of Claim 7 wherein the leads are arranged in an inner set which extends at least partially about the die paddle in spaced relation thereto, and an outer set which extends at least partially about the inner set in spaced relation thereto.

9. The semiconductor package of Claim 8 wherein the leads of the inner set and the leads of the outer set are separated from each other by a plurality of isolation trenches formed in the exterior surface of the package body.

10. The semiconductor package of Claim 9 wherein portions of each of the leads of the inner and outer sets are exposed in respective ones of the isolation trenches.

11. The semiconductor package of Claim 1 wherein the leads are arranged in an inner set which extends at least at partially about the die paddle in spaced relation thereto, and an outer set which extends at least partially about the inner set in spaced relation thereto.

12. The semiconductor package of Claim 11 wherein the leads of the inner set and the leads of the outer set are separated from each other by a plurality of isolation trenches formed in the exterior surface of the package body.

13. The semiconductor packager of Claim 12 wherein portions of each of the leads of the inner and outer sets are exposed in respective ones of the isolation trenches.

14. The semiconductor package of Claim 1 wherein the semiconductor die is electrically connected to the first surfaces of the leads via conductive wires which are covered by the package body.

15. The semiconductor package of Claim 1 wherein the aperture of the tie bar has a circular configuration.

16. A semiconductor package, comprising:

a quadrangular die paddle defining four corners and opposed, generally planar first and second surfaces;

at least one set of leads extending at least partially about the die paddle in spaced relation thereto, each of the leads defining opposed, generally planar first and second surfaces;

four tie bars attached to and extending diagonally from respective ones of the four corners of the die paddle, each of the tie bars defining opposed, generally planar first and second surfaces and an outer end surface;

a semiconductor die attached to the first surface of the die paddle and electrically connected to at least one of the leads; and

a quadrangular package body having four corners and a recess formed within each of the corners thereof, the package body at least partially covering the die paddle, the leads, the tie bars and the semiconductor die such that the second surfaces of the leads are exposed in and substantially flush with a common exterior surface of the package body, and the outer end surface of each of the tie bars is exposed in a respective one of the recesses of the package body.

17. The semiconductor package of Claim 16 wherein:

each of the recesses defines first and second recess walls; and

portions of the outer end surface of each of the tie bars are exposed in each of the first and second recess walls of a respective one of the recesses.

18. The semiconductor package of Claim 17 wherein the first and second recess walls of each of the recesses extend in generally perpendicular relation to each other.

19. The semiconductor package of Claim 18 wherein:

the die paddle includes an etched surface which circumvents the second surface thereof;

the first surface of each of the tie bars extends in substantially co-planar relation to the first surface of the die paddle; and

the second surface of each of the tie bars extends in substantially co-planar relation to the etched surface of the die paddle.

20. The semiconductor package of Claim 19 wherein:

the first surface of each of the leads extends in substantially co-planar relation to the first surface of the die paddle;

the second surface of each of the leads extends in substantially co-planar relation to the second surface of the die paddle; and

the second surfaces of the leads and the second surface of the die paddle are exposed in and substantially flush with the exterior surface of the package body.

21. The semiconductor package of Claim 20 wherein the leads are arranged in an inner set which extends at least partially about the die paddle in spaced relation thereto, and an outer set which extends at least partially about the inner set in spaced relation thereto.

22. The semiconductor package of Claim 21 wherein the leads of the inner set and the leads of the outer set are separated from each other by a plurality of isolation trenches formed in the exterior surface of the package body.

23. The semiconductor package of Claim 22 wherein portions of each of the leads of the inner and outer sets are exposed in respective ones of the isolation trenches.

24. The semiconductor package of Claim 16 wherein the semiconductor die is electrically connected to the first surfaces of the leads via conductive wires which are covered by the package body.